# **Department of Computer Science and Engineering**

### **BRAC University**

### **CSE 260: Digital Logic Design**

# **Experiment #** 3

## ***Parity Generator and Checker***

**Objective:**

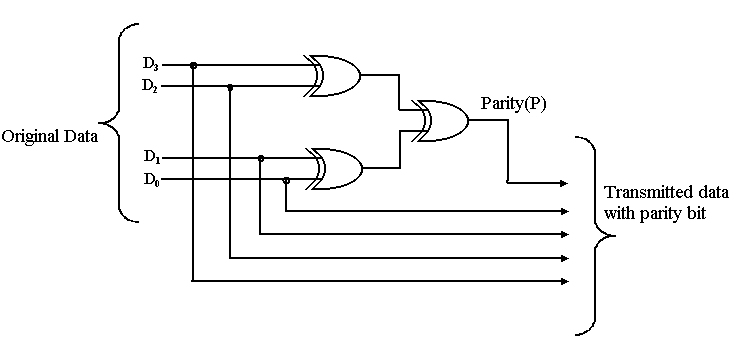
* To design and implement an Even parity Generator and Even parity checker using XOR gates) (IC-7486).

**Required Components and Equipments**

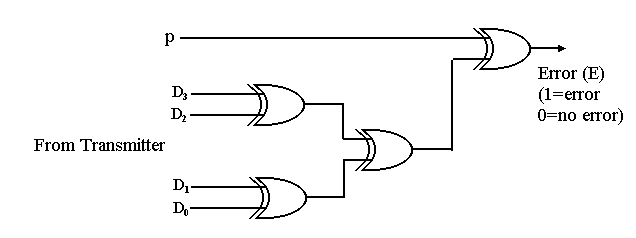
1. AT-700 Portable Analog/Digital Laboratory
2. 7400×3

**Diagram of Circuit:**

#### **Even Parity generator**



**Even Parity Checker**



**Procedure:**

* Construct the Circuit of Figure 1, on the breadboard of AT-700.
* Remember each IC’s pin 14 connected to “+5V” position of DC Power Supply of AT-700, and pin 7 connected to “GND” position.
* Connect the inputs to Data switches and outputs to any position of LED Display.
* Determine the parity generator’s output for each of the following sets of input data, D3D2D1D0; (a) 0111; (b) 1001; (c) 0000; (d) 0100
* Determine the parity checker’s output for each of the following sets of data from the transmitter

**P D3 D2 D1 D0**

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0 1 0 1 0

1 1 1 1 0

1 1 1 1 1

1 0 0 0 0

***Report:***

The report should cover the followings

1. Name of the Experiment
2. Objective
3. Required Components and Equipments
4. Experimental Setup (You must draw the diagrams)
5. Results in Tabulated form.
6. Discussions (Explanation of the results)